Robust Connectivity Solutions for Next-Generation Automotive Data Networks

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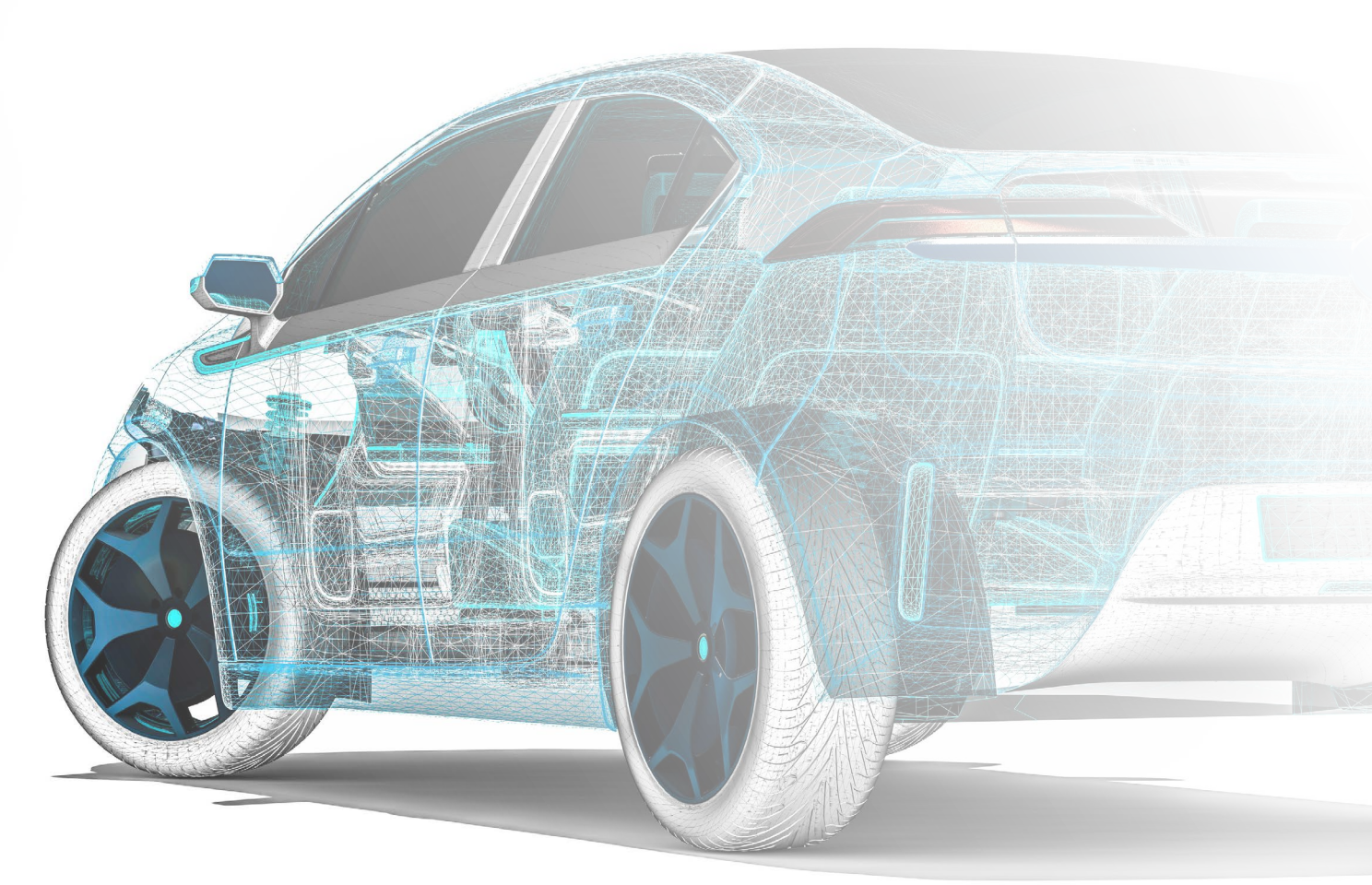
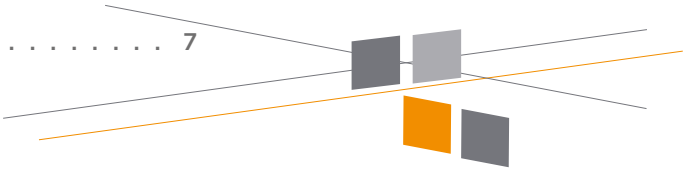


Content



1. Executive Summary

New architectures incorporating high-speed computing clusters supporting signal processing for applications based on sensor fusion will have increasingly challenging requirements for data communications within vehicles.

With the evolution towards autonomous driving and the greater number of automated driving functions within the vehicle, high-speed data transmission lanes in vehicles are becoming increasingly relevant to the safety of the vehicle. This means that new design features for vehicle components are required and that OEMs must consider the limitations of physical channel properties during the definition of the architecture and the selection of the communication protocol.

This white paper discusses the impact of the new architecture approaches on data communication link requirements. It presents an analysis of the trade-off between chip implementation complexity and channel performance limitations and evaluates the maximum reachable data-rates under established automotive conditions. It also describes new connector component design features that are required for this new generation of high speed data-dependent safety critical applications.

2. Introduction: The Next Generation of Automotive Architectures.

Fragmented vs. Converged Architectural Approach

A modern luxury vehicle can contain up to 100 electronic control units (ECUs) based on multiple proprietary operating systems. These range from simple control programs to complex, real-time, multifunctional operating systems or embedded platforms that support, for example, increasingly sophisticated infotainment and driver assistance systems.

The number and complexity of advanced driver assistance systems (ADAS) that will ultimately lead to fully automated driving is increasing.

As a result, traditional ECU-based architectures are reaching their limits. OEMs therefore require the development of new concepts to manage the high levels of complexity and data through-put.

By clustering functions into domains and converging ECUs, OEMs can optimize the weight of the harness and reduce connectivity complexity. This could result in a reduction in the number of components needed and the overall cost. The difference between the classical fragmented architecture approach and the new converged architecture is illustrated in *Fig. 1*.

Service-oriented Architectures

In terms of high-speed data connectivity and computing performance, the integration of ADAS applications is one of the most significant challenges facing OEMs when designing vehicle architectures. High-resolution cameras and

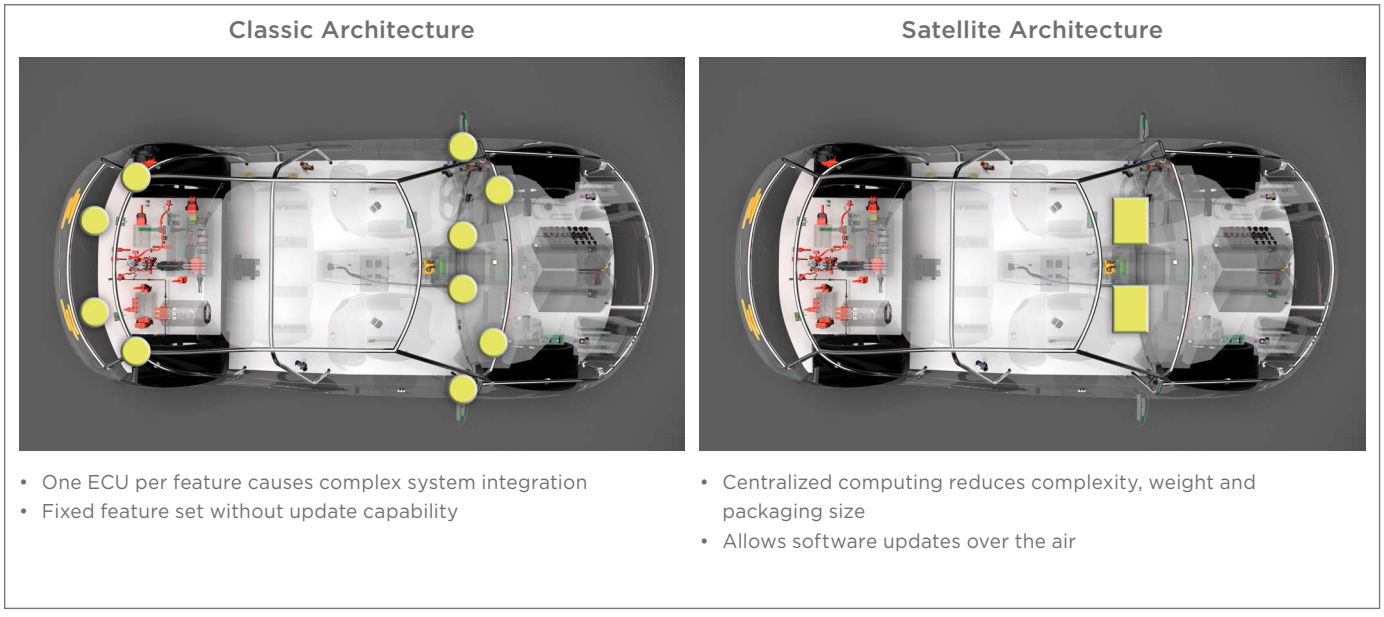


Figure 1: Classic Architecture vs. Satellite Architecture

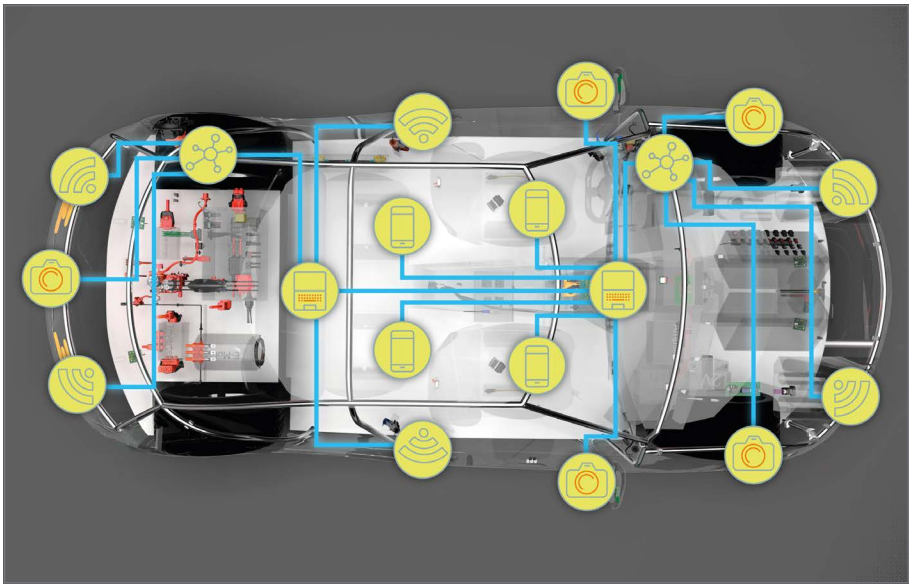


Figure 2: Networking technologies

high performance sensors such as RADAR and LIDAR generate and require an immense amount of data.

Within the vehicle, that data must be transmitted over several meters and processed by powerful computing systems. For safety reasons, the ADAS cluster features a redundant computing platform. High-priority ADAS data is also transferred to a secondary computing platform that is physically separated from the ADAS system. In the event of a complete ADAS breakdown, this data can be used to activate an emergency-mode to bring the vehicle safely to a stop.

Fig. 2 depicts a blend of different networking technologies that may be featured in a next generation vehicle data networking architecture. As the primary control units, the high-speed computing domains require a symmetrical, robust, easy-to-implement and standardized networking technology with high-performance backbone connectivity such as Ethernet.

Cameras and displays usually need asymmetrical links with one-directional high-speed data rates. For these connections, less complex physical layers consisting of a serializer and a de-serializer chipset have become established in recent years.

Generally, other sensors and actuators require much lower data rates, which enable the use of more cost-effective and very established bus technologies like CAN(-FD) or LIN. Gateways, that enable the data transfer between the different network technologies and protocols will play an important role in these new architecture concepts.

3. Communication Technologies within Next-Generation Vehicles

Heterogenic high-speed chip landscape and standardization trends

For a number of years, Ethernet has been deployed in vehicles to enable diagnostics and to support infotainment systems. By adding deterministic timing functions, the application spectrum of Ethernet can be significantly expanded. For example, in order to reduce costs, Ethernet can be used as a network backbone medium for inter-domain controller networks and to replace existing serial networks such as MOST and FlexRay.

Ethernet offers flexibility in architectural design and supports line, star, and hybrid ECU connection structures. As such, it was considered a promising candidate for many topology configurations in automotive applications.

However, since the original Ethernet standards were not created for time or safety-critical applications, their adaptation to automotive applications has been the subject of several working groups within the Institute of Electrical and Electronics Engineers (IEEE) to add features especially for automotive environments.

Initially Ethernet cables, for use in buildings, were very thick, double-shielded, and rather inflexible. Subsequently, Ethernet has become attractive to the automotive market, due to the recent use of more lightweight and cost-efficient unshielded twisted-pair cables.

100BASE-T1 Ethernet technology with a maximum data rate of 100 Mbps was introduced and promoted by BroadR-Reach. This received further support from the OPEN Alliance Special Interest Group, including different OEMs as well as ECU, chip and connector suppliers. Possible applications for **100/1000BASE-T1** are connections to rear-view cameras with a 360-degree panoramic view, RADAR and LIDAR based systems for collision avoidance as well as driver cockpit systems and infotainment solutions.

Soon, 1 Gbps **(1000BASE-T1)** will be implemented, enabling higher application performance. TE Connectivity's MATEnet portfolio of connectors offers a solution with optimized channel parameters for these Ethernet links.

In 2017 another IEEE working group was created with the target of increasing the automotive Ethernet

data rate to the multi-gigabit range. The NGAUTO working group is developing the multi-gigabit standard (IEEE P802.3ch) for data rates of 2.5, 5 and 10 Gbps on full-duplex shielded differential cables. Current progress on the 10 Gbps Ethernet standard includes a preliminary channel specification.

Based on the available automotive qualified cables as well as channel analysis data contributed by TE as an active participant of the consortium, this specification limits the used channel bandwidth to 4 GHz for return loss and insertion loss and 5.5 GHz for the coupling attenuation.

For high-resolution camera and display connectivity, asymmetrical point-to-point links instead of full-implemented Ethernet consisting of a serializer chip on the transmitter side and a deserializer on the receiver side ("SerDes") have been deployed by OEMs in recent years. The current generation with APIX II, GMSL, FPD III-Link allows data rates of up to 3 Gbps on a single coaxial or differential cable. In 2019-2020, the next generation of this technology will be implemented by OEMs in vehicle architectures for the first time.

OEMs can increase data rates to 6 Gbps on one channel or 12 Gbps, if two channels are combined. Unlike Ethernet, the SerDes protocols are not yet standardized. As a result, chip suppliers are releasing multiple proprietary solutions which are often not compatible with each other. A numbers of OEMs, as well as device and chip manufacturers, have begun to work on standardization, focusing on automotive display and camera links to reduce the number of non-compatible SerDes variants on the market.

The SerDes ICs usually support both coaxial and differential cables for cameras and displays. In contrast to Ethernet, a SerDes system provides an asymmetrical link, which means that the data rate in one direction (downstream channel) is much higher than in the other direction (upstream channel). For these types of applications, this is sufficient as cameras are a source of high-speed data, but only receive control signals with much lower data-rates. Display units, on the other hand are receivers of high-speed data but are only required to send control signals to the ECU, for example in case of touchscreen functionality.

This asymmetric approach reduces physical complexity and the channel requirements regarding return loss. As a result, OEMs can create a system that is more cost-effective and tailored to the application than a full-duplex Ethernet-based implementation with the same data rates. For these reasons it is likely that next generation architectures will feature both Ethernet and SerDes.

TE Connectivity is working closely with chip suppliers of the established SerDes system and we track the progress of the standardization process. This enables us to adapt rapidly our product portfolio to the specified channel data for upcoming data communication protocols.

System performance based on chip implementation and channel

Fig. 3 illustrates a full data communication system, consisting of the channel and the transceiver chipsets (integrated circuits, ICs) within the physical layer (PHY). The channel contains two headers (PCB connectors) and various cable segments, depending on the link topology, that are connected via inline-connectors. The maximum available data rate of the system depends on a combination of chip and channel complexity.

If there is the goal to reduce chipset costs, size, and power consumption, a simple modulation (e.g. Pulse-Amplitude-Modulation with two amplitude levels, PAM-2) could be used to reduce complexity of equalization, filtering, or digital signal processing. However, to realize high data rates with such low-complex implementation, this approach requires broadband channels with low attenuation and smooth frequency response over a large bandwidth.

System suppliers often encounter situations where channels provide only limited bandwidth, non-linearities of frequency response, or strong echoes caused by channel components. Such sub-optimal scenarios can be addressed with additional implementation complexity at the chip level.

All parties of the complete system development consortium must therefore analyze the trade-off between chip and channel complexity in order to identify a balanced solution for an optimized system for the target data rate. As an example, TE Connectivity and the Fraunhofer Institute IIS have conducted an analysis of channel capacity based on automotive requirements such as topologies featuring link lengths of 10-15 m, EMI performance, signal integrity and IC implementation limitations.

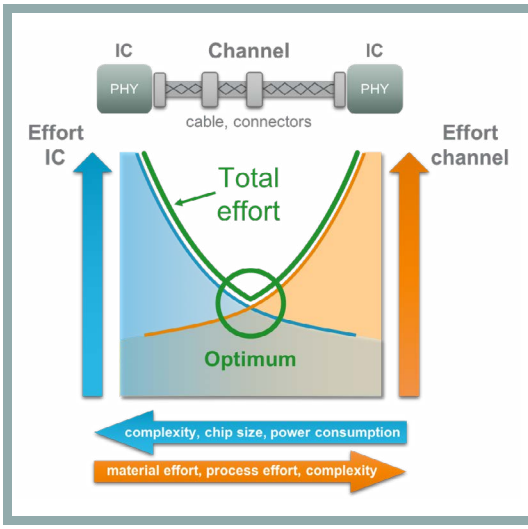


Figure 3

The goal of this study was to evaluate maximum data rates of available automotive channels. The results are presented in sections 4 and 5 below.

4. Connectors Robustness for High-Performance Channel Design

As the functionality levels of ADAS systems become more sophisticated, the performance and reliability of data links to cameras and sensors becomes increasing significant.

real system performance. Therefore, it is increasingly important that component developers conduct a robustness assessment that considers all critical tolerances. Furthermore, the lower link budgets due to the larger required bandwidth cause limited degrees of freedom when designing architectures regarding component choice and maximum link lengths.

Figure 5 shows an example of a typical automotive Ethernet link. The measured channel performance under ideal laboratory conditions on

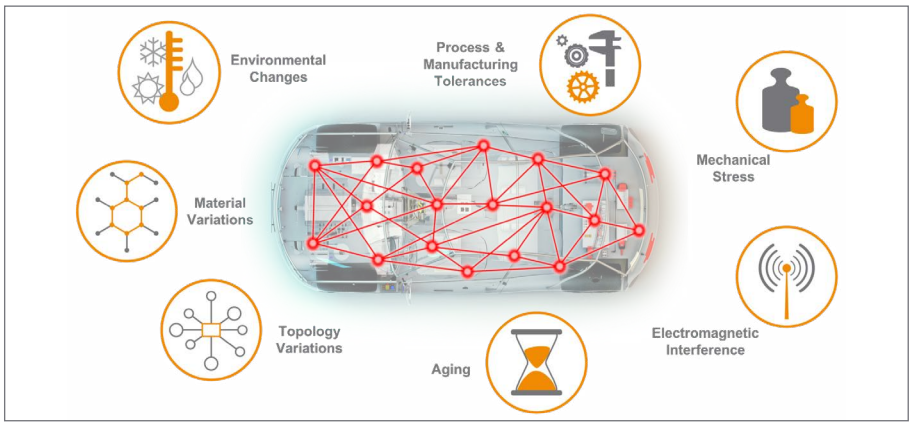


Figure 4

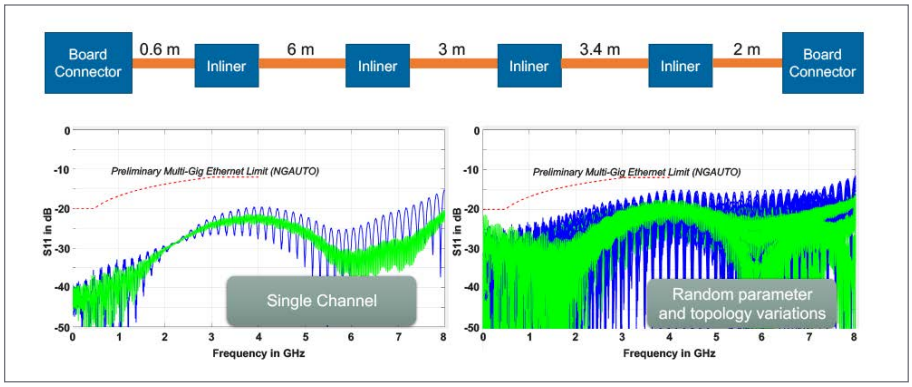


Figure 5

At the same time, higher data rates exploit the full data capacitance of the communication links and more complex physical implementations on chip side. As market demands continue to push solutions close to their physical limitations, there is a lower margin between limit lines and the left side is a good example that demonstrates the high margin level between link performance and the application limit line.

However, when all component tolerances (e.g. cable and connector impedance) and environmental effects (e.g. temperature effects, humidity, aging) are considered, the margin is highly decreased as shown by the array of curves on the right side. It is therefore critical that all these system parameters are considered in combination with each other already during the system design process to fulfill the application requirements even in a absolute worse-case scenario where all these effects have been taken into account.

5. Limitations of available Channel Bandwidth and Lengths

Since the required maximum data-rates of upcoming new and improved applications in future automotive architectures are not predictable yet, it is important for component suppliers like TE to know the maximum achievable data-rates with established automotive technologies.

In order to calculate the maximum achievable data rate on the communication channel, we use the Shannon-Hartley data capacity definition theorem, as shown in the following equation:

$$(1)\quad C = BW \log_2(1 + S/N)$$

This expression describes the data capacity (C) of a channel in bit/s, with Gaussian white noise as a given frequency bandwidth (BW) based on the signal (S) and noise (N) power. We are able to calculate the data capacity for real channels with a noise power distribution different from Gaussian white noise, by normalizing equation (1) to the bandwidth resulting in the data capacity density (C') in bit/s/Hz shown in equation (2) below.

$$C' = \frac{C}{BW} = \log_2\left(1 + \frac{S}{N}\right) = \log_2\left(1 + \frac{PD\,Tx_{shaped} \cdot IL}{PD_{EMI} \cdot TF_I + PD\,N + PD\,Tx_{up} \cdot RL}\right) = \log_2\left(1 + \frac{PD\,Tx_{shaped}}{PD\,N_{total}}\right) \qquad (2)$$

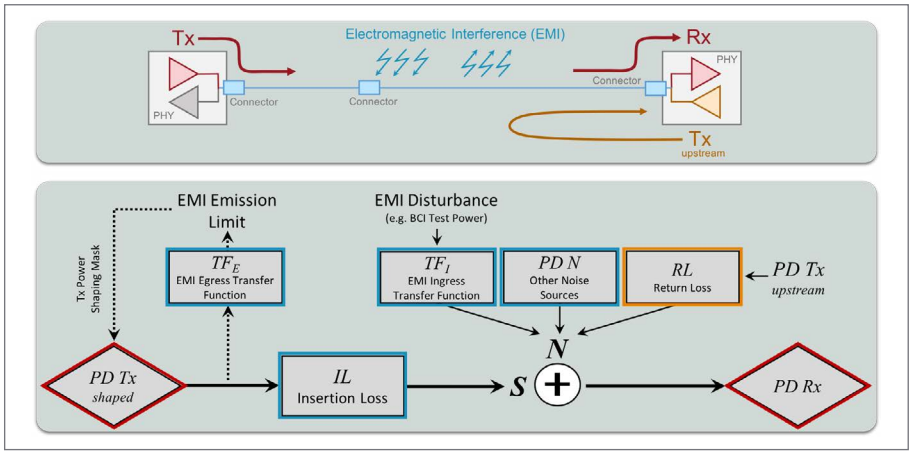


Figure 6

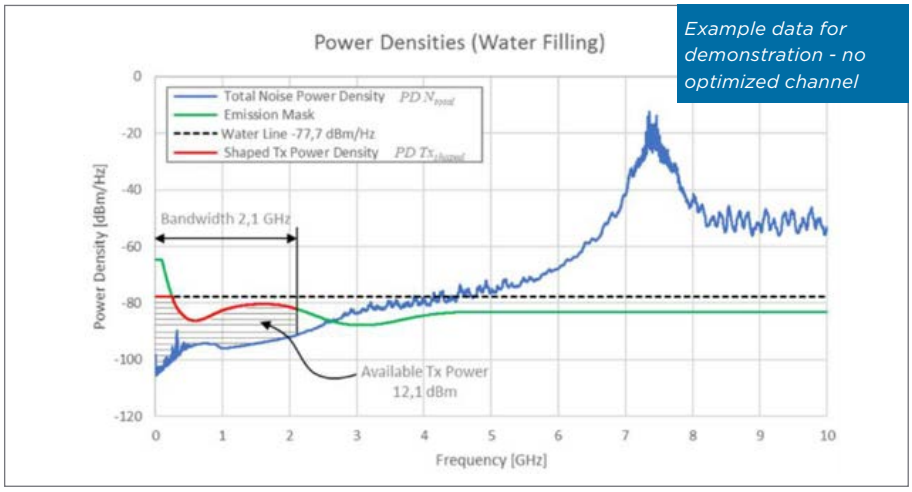


Figure 7

The signal-to-noise ratio can then be calculated numerically for discrete frequency bandwidth steps that are small enough to assume the Gaussian white noise within. The basis for this calculation is the channel model shown in *Fig. 6.*

The total noise power density (PDN_{total}) is the sum of all disturbances. External EMI sources (PD_{EMI}), the upstream signal (PD Tx_{up}) in duplex operation mode and other disturbances (PDN), such as receiver noise, were considered in the current study. The channel insertion loss function (IL) can also be included inversely within the total noise power density.

In this way, the data capacity density can comfortably be calculated with the shaped transmitter signal power density (PD Tx_{shaped}) and the total noise.

The shaped transmitter signal power density can be determined by using the water filling algorithm (1) as illustrated in *figure 7.*

Beginning at the lowest level, this iterative method attempts to identify the power density function by distributing the available transmitter (Tx) power in a way that exceeds the noise power. This process can be compared to filling a pond with water, whereby the noise power density is marked as the bottom of the pond. The algorithm is completed when all the available power is exhausted. In this study, an EMI emission mask is used as an additional constraint to ensure that automotive EMI requirements are fulfilled.

The mask marks the maximum transmitter power density allowed for the water-filling algorithm. It is calculated by dividing the automotive emission limit by the EMI egress transfer function (TF_E). The diagram in *Fig. 7* provides an illustration of the algorithm.

The total available transmitter power depends on the maximum driver voltage and the channel impedance. 3.3 V CMOS technology and 100 Ohms impedance for differential signaling or 50 Ohms for coaxial cables are used to conduct the data capacity analysis. System developers must consider additional margin needs in duplex operation mode to ensure that the superposition of the transmitted (downstream) voltage and the received (upstream) signal does not exceed the supply voltage.

A representative calculation for 12.1 dBm average transmitter power results in 2.5 V peak on a 100 Ohms differential pair cable. The ratio between peak and average (rms) power depends on the modulation format and was estimated to be 6 dB. This peak voltage still allows duplex operation with asymmetric data rate and reduced transmitter power in the opposite direction. In this example, in order to reflect existing use cases that require a low data rate reverse channel, we assumed that the ratio between the upstream and downstream data rate of 1:20 also existed for the simplex transmission mode.

The example in *Fig. 7*, shows the distribution of the total available transmitter power above the noise power density (blue curve) in a bandwidth of 2.1 GHz. The emission mask acts as an upper limit. The result is the shaped transmitter power density (red curve). A maximum power density of -77.7 dBm/Hz was reached in the lower frequency ranges when the available power was exhausted.

Now we are able to calculate the total data capacity by finding the integral of the data capacity density over the analyzed frequency bandwidth (9.7 Gbit/s for 2.1 GHz bandwidth in the example). This iterative algorithm can then be repeated for increasing bandwidths, resulting in the data capacity versus bandwidth plot as shown in *Fig. 8.*

The achievable data rate of the shown example channel increases up to a bandwidth of 2.7 GHz and there is no further capacity gain for higher frequencies. The main reason is the increasing insertion loss of the cable as it would require more power at the transmitter than is available to use the higher frequencies for data transmission.

The maximum usable frequency and the achievable data rate on copper media is determined by the available transmitter power and the attenuation caused by the cable insertion loss as well as the link length. The analyzed example channel with 0.14 mm^2 stranded wires allow 10 Gbit/s in a simplex operation mode up to a length of 10 m.

Cables with lower attenuation would be required for a duplex operation or for an increased length of 10 m up to 15 m. The maximum usable frequency did not exceed 4 GHz for the analyzed cases. This requires more complex data encoding with multilevel pulse amplitude modulation (PAM) for the implementation of PHY chips. OEMs can increase the achievable data rate to ~20 Gbit/s if they accept a reduced channel length for the specific application they are testing. Such channels would also allow less complex PHY chips using two level PAM for data rates of 10 to 12 Gbit/s.

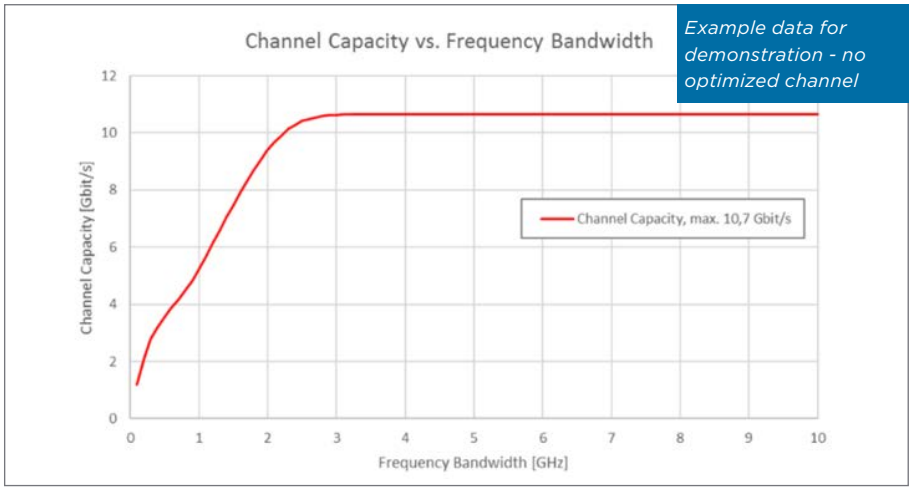


Figure. 8

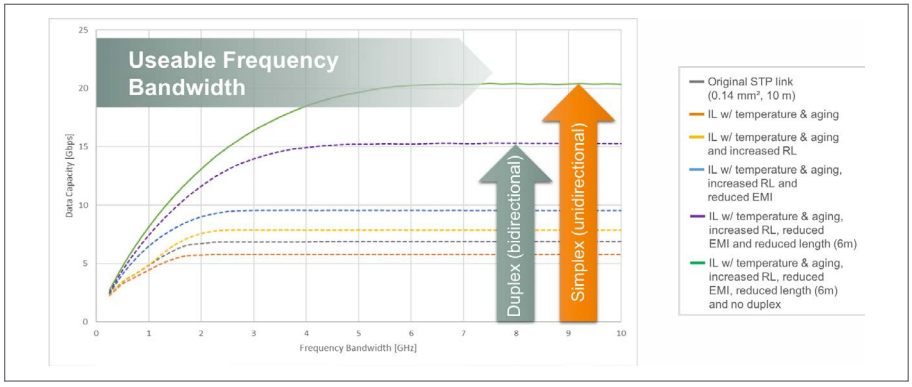


Figure 9

The limiting parameter from the connector point of view is the return loss. The data rate for a duplex operation is reduced significantly if the reflections are too high. The simulations indicate a required connector return loss greater than 15 to 20 dB within the used operating frequency bandwidth, with relaxation permitted in case of simplex operation.

This is potentially an interesting option for dual lane applications where upstream and downstream data use separate links. It also allows OEMs to use simpler, more affordable PHY chipsets. Connectors supporting multiple lanes for one channel are needed in this scenario. This study has also shown significant dependence of the achievable data rate on EMI requirements. Fully shielded cables and connectors with coupling attenuation in the region of -60 dB or better are needed for this reason.

The analysis was limited to baseband signaling on typical STP cables. Coaxial cables can have significant lower insertion loss compared to STP cables of same diameter. However, there are reasons related to the EMI design of ECUs, to the grounding concept and to system cost that justify specific use cases for both alternatives in automotive applications.

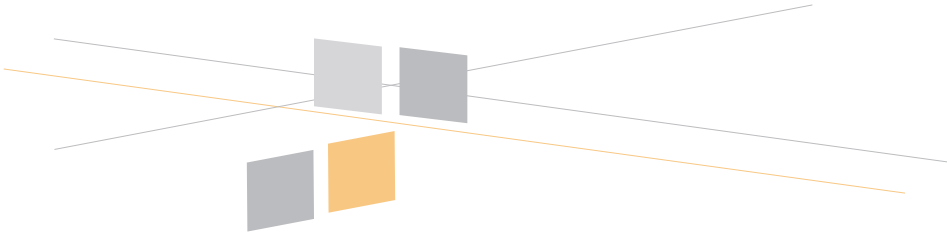
These analysis results for different channel parameters are summarized in Fig. 9.

Conclusion

In summary, it can be concluded that the useable frequency bandwidth stays below 10 GHz for typical automotive cabling. With an adapted modulation scheme on chip side a data rate of approximately 20 Gbit/s on single STP lane is possible depending on cable type and link length (see *Fig. 9*).

However, it is clear that the performance requirements of future systems will stretch automotive channels to their physical limitations. That means designers of in-vehicle data networks architectures need to carefully consider the appropriate cable types, link lengths and choice of connectors.

TE Connectivity is using these performance benchmarks as the design principles for its data connectivity portfolio for next generation architectures. We are collaborating with OEMs and chip manufacturers to design connectors specifically to address the next generation architecture high-speed data needs. This includes supporting one- to multi-Gbps links deployments for centralized data back-bones, transporting raw uncompressed data from new cameras and sensors that will support the upcoming level 4 and 5 autonomous driving applications as well as the most advanced in-vehicle infotainment experiences.



Footnotes

(1) https://en.wikipedia.org/wiki/Water_filling_algorithm

About TE Connectivity

TE Connectivity Ltd. (TE) is a $14 billion global technology and manufacturing leader creating a safer, sustainable, productive, and connected future. For more than 75 years, our connectivity and sensor solutions, proven in the harshest environments, have enabled advancements in transportation, industrial applications, medical technology, energy, data communications, and the home.

With 80,000 employees, including more than 8,000 engineers, working alongside customers in approximately 140 countries, TE ensures that EVERY CONNECTION COUNTS. Learn more at **www.te.com** and on **LinkedIn**, **Facebook**, **WeChat** and **Twitter**.

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